

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the Application:

LISTING OF CLAIMS:

1. (Currently Amended) A testing device for testing a plurality of peripheral devices, each of said plurality of peripheral devices being equipped with a USB interface, comprising:
 - a CPU;
 - a memory including a predetermined firmware program, said memory being connected directly to said CPU; and
 - a control chip including a USB interface control having a plurality of connecting ports for connecting directly with said plurality of peripheral devices under ~~the~~ test for proper actual operation, said control chip being coupled to said CPU;wherein said firmware program of said memory controls said CPU to test said plurality of peripheral devices under ~~the~~ test through said control chip.
2. (Original) The device of claim 1, wherein said memory is provided with a test packet.

3. (Currently Amended) The device of claim 2, wherein said CPU sends said test packet to said plurality of peripheral devices under ~~the~~ test through said control chip.
4. (Currently Amended) The device of claim 3, wherein, after receiving said test packet, each of said plurality of peripheral devices under ~~the~~ test sends back said test packet to said CPU for determining whether said test packet is the same as a predetermined said test packet provided in the memory.
5. (Currently Amended) A testing device for testing ~~of~~ at least one peripheral device, wherein said at least one peripheral device is provided with a USB interface, said testing device comprising:
- a CPU having a memory with a predetermined firmware program inside said CPU; and
 - a control chip with USB interface, said control chip being connected to said CPU ;
- wherein said control chip is provided with a plurality of connecting ports for connecting directly with said at least one peripheral device under ~~the~~ test to test for proper actual operation of said at least one peripheral device.

6. (Previously Presented) The device of claim 5, wherein said memory further includes a test packet .
7. (Currently Amended) The device of claim 6, wherein said CPU sends said test packet to said at least one peripheral device under the test through said control chip.
8. (Currently Amended) The device of claim 7, wherein, after receiving said test packet, said at least one peripheral device under the test sends said test packet back to said CPU for determining whether said test packet is the same as predetermined said test packet provided in the memory.
9. (Currently Amended) A testing device for testing of at least one peripheral device, wherein said at least one peripheral device is provided with USB interface, comprising ~~characterized by~~:
 - a CPU directly connected with at least one memory, said memory comprising a firmware program for ~~indicating~~ controlling said CPU;
and
 - a control chip with USB interface control, said control chip being connected to said CPU;

wherein said CPU sends a test packet stored in the memory to said at least one peripheral device under the test through said control chip to test for proper actual operation; and

wherein, after receiving said predetermined test packet, said at least one peripheral device under the test sends said test packet back to said CPU for determining whether said test packet is the same as a predetermined said test packet stored in the memory.